In the Claims:

1. (Currently Amended) A semiconductor device, comprising:

a gate electrode on a semiconductor substrate, the gate electrode including a metal silicide layer on a polysilicon layer and extending in a first direction;

~~a plurality of isolation regions in the semiconductor substrate that define an active region;~~

~~a gate electrode on the active region, wherein the gate electrode comprises a metal silicide layer on a polysilicon layer;~~ and

a conductive line pattern ~~layer~~ extending in the first direction and being in contact with the gate electrode along the first direction.~~that is on, and electrically connected to, the gate electrode~~;

~~wherein the conductive layer bridges at least one gap in the metal silicide layer.~~

2. (Cancelled)

3. (Currently Amended) The semiconductor device of Claim 1, further comprising a gate insulation pattern between the semiconductor substrate and the gate electrode. ~~the active region and the gate electrode.~~

4. (Cancelled)

5. (Currently Amended) The semiconductor device of Claim 1[[4]], wherein the conductive line pattern is formed of at least one of aluminum, tungsten, titanium, tantalum, or copper.

6. (Currently Amended) The semiconductor device of Claim 1[[4]], further comprising an interlayer dielectric on the semiconductor substrate, and wherein the conductive line pattern is disposed in a groove in the interlayer dielectric.

7. (Currently Amended) The semiconductor device of Claim 6, further comprising a plug line penetrating the interlayer dielectric layer, the plug line being electrically connected

to the semiconductor substrate outside of the gate electrode and extending in the first direction. ~~wherein the interlayer dielectric includes a second groove, and wherein the device further comprises a plug line that electrically connects a source/drain region in the semiconductor device with a source/drain region of an adjacent semiconductor device.~~

8. (Original) The semiconductor device of Claim 1, further comprising a planarized interlayer dielectric on the semiconductor substrate,

wherein the top surface of the planarized interlayer dielectric and the top surface of the gate electrode are substantially the same height above the semiconductor substrate.

9. (Currently Amended) The semiconductor device of Claim 1, further comprising a second gate electrode with the same material as the gate electrode, wherein the conductive line pattern is in contact with the second gate electrode. ~~further comprising a second active region in the semiconductor substrate with a second gate electrode thereon,~~

~~wherein the second gate electrode comprises a metal silicide layer on a polysilicon layer, and~~

~~wherein the conductive layer is a conductive line pattern that electrically connects the gate electrode and the second gate electrode.~~

10. (Currently Amended) The semiconductor device of Claim 9, wherein the second gate electrode extends in the first direction. ~~conductive line pattern is directly on both the gate electrode and the second gate electrode.~~

11. (Currently Amended) The semiconductor device of Claim 9, wherein the second gate electrode extends in a second direction, and wherein the conductive line pattern further extends along the second direction. ~~1, wherein the conductive layer decreases the resistance of the gate electrode.~~

12. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a gate line including a gate insulation pattern and a gate electrode which are sequentially stacked on the semiconductor substrate;

a spacer formed on a sidewall of the gate line; ~~and~~

a conductive line pattern disposed on the gate line; and

an interlayer dielectric on the semiconductor substrate having a top surface that is coplanar with a top surface of the gate line;

wherein the conductive line pattern is parallel to the gate line and electrically connected to the gate electrode.

13. (Original) The semiconductor device of Claim 12, wherein the gate electrode comprises a doped polysilicon layer.

14. (Original) The semiconductor device of Claim 13, further comprising a metal silicide layer, wherein the metal silicide layer is on the doped polysilicon layer.

15. (Original) The semiconductor device of Claim 14, further comprising an interlayer dielectric on the semiconductor substrate that includes a groove that exposes a top surface of the gate line, and wherein the conductive line pattern is provided in the groove.

16. (Original) The semiconductor device of Claim 15, further comprising an etch-stop layer between the semiconductor substrate and the interlayer dielectric, wherein the etch-stop layer has an etch selectivity with respect to the interlayer dielectric.

17. (Cancelled)

18. (Original) The semiconductor device of Claim 12, wherein the conductive line pattern has at least the same length as the gate line.

19. (Original) The semiconductor device of Claim 12, wherein the conductive line pattern is made of metal.

20. (Original) The semiconductor device of Claim 14, wherein the conductive layer

bridges at least one gap in the metal silicide layer.

21. (Original) The semiconductor device of Claim 12, wherein the conductive layer decreases the resistance of the gate electrode.

22. (Original) A semiconductor device comprising:

a semiconductor substrate;

a first gate line and a second gate line on the semiconductor substrate and spaced apart from each other, the first gate line including a first gate electrode stacked on a first gate insulation pattern, and the second gate line including a second gate electrode stacked on a second gate insulation pattern; and

a conductive line pattern on the first and second gate lines, wherein the conductive line pattern has a first portion parallel to the first gate line and a second portion parallel to the second gate line, and wherein the conductive line pattern electrically connects the first and second gate electrodes with each other.

23. (Original) The semiconductor device of Claim 22, wherein the first and second gate lines comprise a doped polysilicon layer.

24. (Original) The semiconductor device of Claim 23, wherein the first and second gate lines further comprise a metal silicide layer on the doped polysilicon layer.

25. (Original) The semiconductor device of Claim 22, further comprising a spacer disposed on a sidewall of the first and second gate lines and an interlayer dielectric covering the semiconductor substrate that includes a groove that exposes top surfaces of the first and second gate line; and

wherein the conductive line pattern is disposed in the groove in the interlayer dielectric.

26. (Original) The semiconductor device of Claim 25, further comprising an etch-stop layer between the semiconductor substrate and the interlayer dielectric, wherein the etch-

stop layer has an etch selectivity with respect to the interlayer dielectric.

27. (Original) The semiconductor device of Claim 22, further comprising an interlayer dielectric on the semiconductor substrate that is planarized to the height of the first and second gate lines.

28. (Original) The semiconductor device of Claim 22, wherein the first portion of the conductive line pattern is at least the same length as the first gate line, and the second portion of the conductive line pattern is at least the same length as the second gate line.

29. (Original) The semiconductor device of Claim 22, wherein the conductive line pattern is made of metal.

30. (Original) The semiconductor device of Claim 24, wherein the conductive layer bridges at least one gap in the metal silicide layer.

31. (Original) The semiconductor device of Claim 22, wherein the conductive layer decreases the resistance of the gate electrode.

32-45. (Canceled).

46. (New) The semiconductor device of Claim 7, further comprising a second gate electrode on the semiconductor substrate, wherein the second gate electrode comprises a metal silicide layer on a polysilicon layer, and wherein the conductive line pattern electrically connects the gate electrode and the second gate electrode.

47. (New) The semiconductor device of Claim 8, further comprising a second gate electrode on the semiconductor substrate, wherein the second gate electrode comprises a metal silicide layer on a polysilicon layer, and wherein the conductive line pattern electrically connects the gate electrode and the second gate electrode.

48. (New) The semiconductor device of Claim 9, further comprising an interlayer

dielectric on the semiconductor substrate, and wherein the conductive line pattern is disposed in a groove in the interlayer dielectric.

49. (New) The semiconductor device of Claim 48, wherein the interlayer dielectric includes a second groove, and wherein the device further comprises a plug line that electrically connects a source/drain region in the semiconductor device with a source/drain region of an adjacent semiconductor device.